

PATENT APPLICATION

Sheet 1 of 4

<p>FORM PTO-1449</p> <p>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</p> <p>(Use several sheets if necessary)</p>	<p>ATTY. DOCKET NO. 200312380-1</p>	<p>APPLICATION NO.</p>	<p>CONFIRMATION NO.</p>
<p>APPLICANT Grebenkemper, John</p>			
<p>FILING DATE April 9, 2004</p>		<p>GROUP</p>	

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
HL	1A	5,065,284	11-12-1991	Hernandez
HL	1B	5,246,817	09-21-1993	Shipley, Jr.
HL	1C	6,444,922 B1	09-03-2003	Kwong
	1D			
	1E			
	1F			
	1G			
	1H			
	1I			
	1J			
	1K			

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1L				
1M				
1N				
1O				
1P				

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

HL	1Q	Eric BENEDICT, PCB DESIGN FOR EMI/EMC COMPLIANCE, July 21, 2000, WEMPEC Seminar, pp 0-48.
HL	1R	PCBs, EE6471 (KR), November 12, 2002, pp. 259-286.
HL	1S	PROTO CIRCUIT INC., MULTILAYER PRINTED CIRCUIT BOARD PRIMER.

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DATE CONSIDERED

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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

HA	2Q	Mehdi M. MECHAIK, Ph.D., EFFECTS OF PACKAGE STACKUPS ON MICROPROCESSOR PERFORMANCE, pp. 1-7, Computer Aided Engineering & PCB Design Cisco Systems, San Jose, CA.
HA	2R	Minjia XU, Yun Ji, Todd H. HUBING, Thomas P. VAN DOREN, James L. DREWNIK, DEVELOPMENT OF A CLOSED-FORM EXPRESSION FOR THE INPUT IMPEDANCE OF POWER-GROUND PLANE STRUCTURES, IEEE, 2000, PP. 77-82.
HA	2S	John B. HOWARD, PCB DESIGN FOR EMC CONTROL CLOCKS AND POWER PLANES, pp. 5B-1 - 5b-13, IEEE Santa Clara Valley EMC '94.

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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

<i>tea</i>	3Q	Jason CONG, Patrick H. MADDEN, PERFORMANCE DRIVEN MULTI-LAYER GENERAL AREA ROUTING FOR PCB/MCM DESIGNS, pp. 356-361.
<i>tea</i>	3R	Jiunn-Nan HWANG, Tzong-Lin WU, COUPLING OF THE GROUND BOUNCE NOISE TO THE SIGNAL TRACE WITH VIA TRANSITION IN PARTITIONED POWER BUS OF PCB, PP. 733-736, IEEE 2002.
<i>tea</i>	3S	Jun FAN, James L. KNIGHTEN, Norman W. SMITH, Ray ALEXANDER, THE EFFECTS OF SIGNAL LAYER POSITIONS IN MULTI-LAYER PCB DESIGNS, PP. 320-324, IEEE 2002.

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<i>ten</i>	4Q	Minjia XU, Todd H. HUBING, Juan CHEN, Thomas P. VAN DOREN, James L. DREWNIK, Richard E. DUBROFF, POWER-BUS DECOUPLING WITH EMBEDDED CAPACITANCE IN PRINTED CIRCUIT BOARD DESIGN, pp. 22-30, IEEE 2003, Vol. 45, No. 1, February 2003.
<i>ten</i>	4R	Sean MERCER, Ph.D., C. Eng., MINIMIZING RF PCT ELECTROMAGNETIC EMISSIONS, pp. 46, 48, 55-56, www.rfdesign.com, January 1999.
<i>ten</i>	4S	Dallas A. DEAN, SILENCE IS GOLDEN 8 WAYS TO REDUCE NOISE ON YOUR NEXT PCB, pp. 15-17, CMP Media LLC, January 1999.

<p>EXAMINER <i>Hoang</i></p>	<p>DATE CONSIDERED <i>7/27/06</i></p>
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